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10/742,938	12/23/2003	Vasu J. Bibikar	42339-198342	7156

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EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/742,938	BIBIKAR ET AL.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *6-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1 – 5 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claim limitations are directed to a data structure (a register comprised of various fields) which constitute non-functional descriptive material therefore a data format which is non statutory.

To expedite a complete examination of the instant application, the claims rejected under 35 U.S.C. 101 (non-statutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claims 1, 2, 3 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The apparatus describes only a data structure (registers). It is unclear how this data structure can perform the data transferring function as intended in the preamble.

To expedite a complete examination of the instant application, the claims rejected under 35 U.S.C. 112 above are best interpreted as a register comprising additional registers for claim 1 and for claims 2, 3 and 5 a direct memory access controller actively performs an operation indicated by bits.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by *Computer Architecture A Quantitative Approach* (hereinafter "Hennessy").

7. As to claim 1, Hennessy teaches an apparatus for data transfer comprising:

a direct memory access register (DRAM is adapted to hold multiple registers, page 103 and 441) to hold a descriptor (descriptor, page 454), said register comprising:

a command register (command register format can be seen on page 99) comprising a single compare enable bit (compare enable bit is the bit storing the

condition for the branching, page 102) and a single branch enable bit (single branch enable bit is the bit storing the opcode for branching, page 102);

a source address register (R4, table 2.24, page 102);

a target address register (name, table 2.24, page 102, target address elaborated on page 276); and

a descriptor address register (descriptor table, page 454, figure 5.45 page 455).

Examiner notes page 99 of Hennessey for better understanding of register structure as well as the branching instructions which a based on single bit values of 1's and 0's which represent true and false for determining branching and comparator results.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hennessy in view of Barry et al. (US Patent Number 6,457,073 hereinafter "Barry").

10. As per claim 2, Hennessy teaches an apparatus wherein said compare enable bit is adapted to indicate a comparison operation to be performed based on said source

address register and said target address register (branch instructions determined by the opcode, page 99, are based on the target and source, figure 2.24, page 102).

Hennessy does not explicitly teach a comparison operation to be performed by a controller.

Barry teaches comparison operations performed by a direct memory access controller (transfer controller supports branch, column 8, lines 63 – 67 and column 9, lines 1 – 37).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify Hennessy with the above teachings of Barry. One of ordinary skill would be motivated to make such modification in order to have an improved technique for carrying out data transfer functions (column 2, lines 1 – 12).

Examiner directs applicant to the background in order to better understand Barry.

11. As per claim 3, Hennessy teaches an apparatus wherein said branch enable bit is adapted to indicate a branch operation to access another descriptor.

Hennessy does not explicitly teach a branch operation to be performed by a controller.

Barry teaches a branch operation performed by a direct memory access controller (transfer controller supports branch, column 8, lines 63 – 67 and column 9, lines 1 – 37).

It would have been obvious to one of ordinary skill in the art to make such modifications for the same reasons of motivation expressed above in claim 2.

Examiner also provides Okubu et al. (US Patent Number 6,456,390) as extrinsic evidence in order to better understand the nature of descriptors in an environment comprising a DMA Controller, in particular column 2, lines 16 – 31 are noted.

12. As per claim 4, Hennessy teaches conditional branch instructions (figure 3.23, page 164).

Hennessey does not explicitly disclose that the conditional branch stores a bit that describes the compare condition in a status register.

Barry teaches an apparatus further comprising a control status register (WAIT PC REGISTER used for status, figure 4E), said control status register comprising a compare status bit (Bits of Wait PC Register, figure 4E used to compare).

It would have been obvious to one of ordinary skill in the art to make such modifications for the same reasons of motivation expressed above in claim 2.

Examiner also provides *Computer Systems Design and Architecture* (hereinafter "Heuring") as extrinsic evidence in order to better understand possible interpretations of control status registers. Heuring teaches an apparatus further comprising a control status register (condition code register, page 39 - 40), said control status register comprising a compare status bit (bit that describes condition, page 39).

13. As per claim 5, Hennessy teaches an apparatus wherein said branch enable bit is adapted to indicate a branch operation to be performed to access another descriptor based on said compare status bit (branch to segment descriptor, page 454 - 455).

Hennessey does not explicitly disclose a branch operation to be performed by a controller.

Barry teaches a branch operation performed by a direct memory access controller (transfer controller supports branch, column 8, lines 63 – 67 and column 9, lines 1 – 37).

It would have been obvious to one of ordinary skill in the art to make such modifications for the same reasons of motivation expressed above in claim 2.

Response to Arguments

14. Applicant's arguments filed 5/7/2007 have been fully considered but they are not persuasive. Applicant argues:

1) Applicant did not agree with the 35 U.S.C. 101 and 35 U.S.C. 112 rejections and amended the claims to put them in condition overcome the rejections.

2) Hennessy does not teach a single compare enable bit or a single branch enable bit.

15. As per argument 1, the Examiner respectfully disagrees. The newly amended claim limitations "for data transfer" and removal of "adapted to" do not overcome the 35

U.S.C. 101 and 35 U.S.C. 112 rejections. The newly amended claims are directed to a data structure in the form registers which is nonfunctional descriptive material and non statutory. The claim limitation "for data transfer" renders the claims indefinite because it is unclear as to how a data structure can perform the newly amended claim limitations intended in the preamble.

16. As per argument 2, the Examiner respectfully disagrees. The Examiner makes several notes in reference to the Applicant's arguments and how Hennessey is still deemed to be relevant prior art over the currently claim invention. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., compare enable is only one bit and branch enable is only one bit) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claim limitation "a command register **comprising**" necessitates that the invention includes ***at least one*** of the following limitations. Therefore it necessitates that Hennessey contain at least one single compare enable bit and at least one single branch enable bit, which Hennessey clearly discloses on page 102 in the bits for branching and in the opcode itself. The Applicant is further directed to page 99 of Hennessey for better understanding of general register structure and bit usage for instructions.

Assuming arguendo, the Examiner also notes MPEP 2144.04 IV A. Changes in Size/Proportion, see *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955), in which it is expressed that size alone is not a patentable feature. It is known to one of ordinary skill in the art that an instruction has an opcode and a function that is comprised of bits and varying the instruction length is not a novel patentable feature as it has **exactly the same functionality**.

Clearly from the above citation one of ordinary skill in the art would recognize that Hennessey teaches ***at least one*** single compare enable bit and ***at least one*** single branch enable bit.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571) 272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

KIM HUYNH
SUPERVISORY PATENT EXAMINER
7/23/07